



10-Channel Level-Shift with Charge Sharing for GOP Panel

General Description

The LP6297B is a 8-CH high voltage level shifter for TV and monitor LCD applications. It converts logic level signals from Timing Controller (T-CON) to high level signals used by the LCD panel.

The outputs are switching from VGL to VGH, with capacitive loads up to 5nF.

Other features include short circuit protection, thermal shutdown protection and under-voltage lockout (UVLO). The LP6297B is available in a space saving TQFN-32 (0.4mm pitch) package.

Order Information

LP6297 □□□□
 └─ F: Pb-Free
 └─ Package Type
 BQV: TQFN-32



Features

- ◆ -20V to 40V High Output Level
- ◆ Support Two Kinds of TCON Input Signals
 - TCON Mode 0
 - TCON Mode 1
- ◆ High Output Slew Rate to Drive Up to 5nF Load
- ◆ Over Current Protection
- ◆ Over Temperature Protection
- ◆ Available in TQFN-28 (4x4mm)
- ◆ Available in TQFN-32 (4x4mm)
- ◆ RoHS Compliant and Halogen Free
- ◆ Pb-Free Package

Applications

- ◆ TFT for NB Using GOP/IPS Technology
- ◆ TFT for Monitors Using GOP/IPS Technology
- ◆ TFT for TV Using GOP/IPS Technology

Marking Information

Device	Marking	Package	Shipping
LP6297B	LPS LP6297B YWX	TQFN-32	3K/REEL

Y: Y is year code. W: W is week code. X: X is series number.



Typical Application Circuit

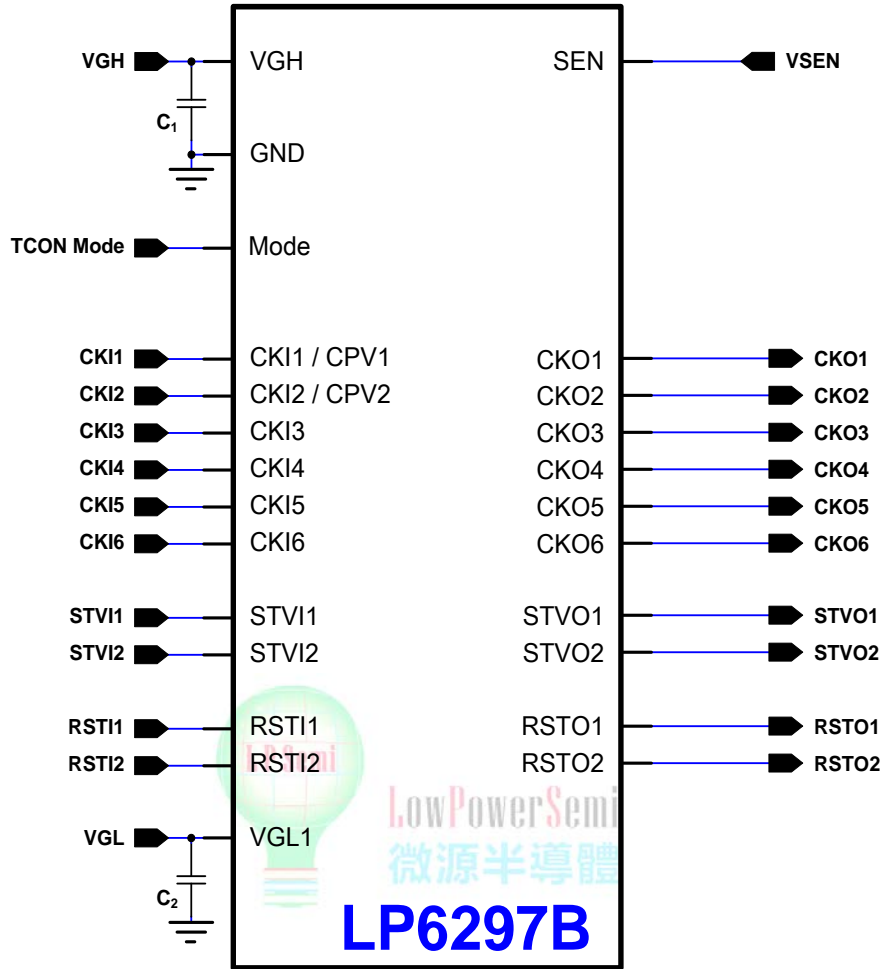


Figure 1. Typical Application Circuit of LP6297B



Pin Configuration

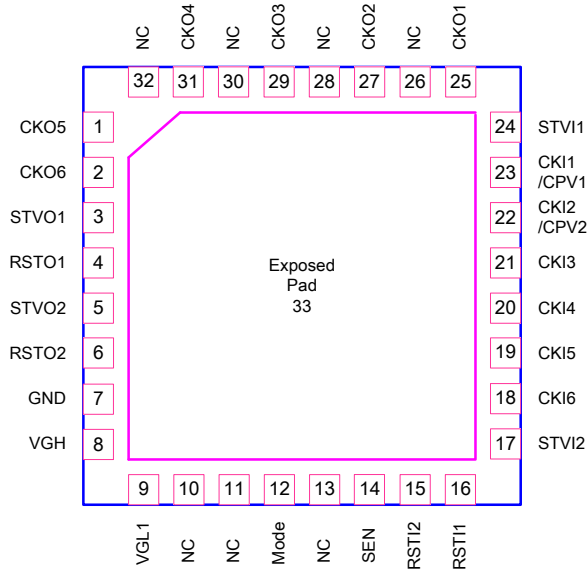


Figure 2. TQFN-32 Package (4mm x 4mm) Top View





Function Block Diagram

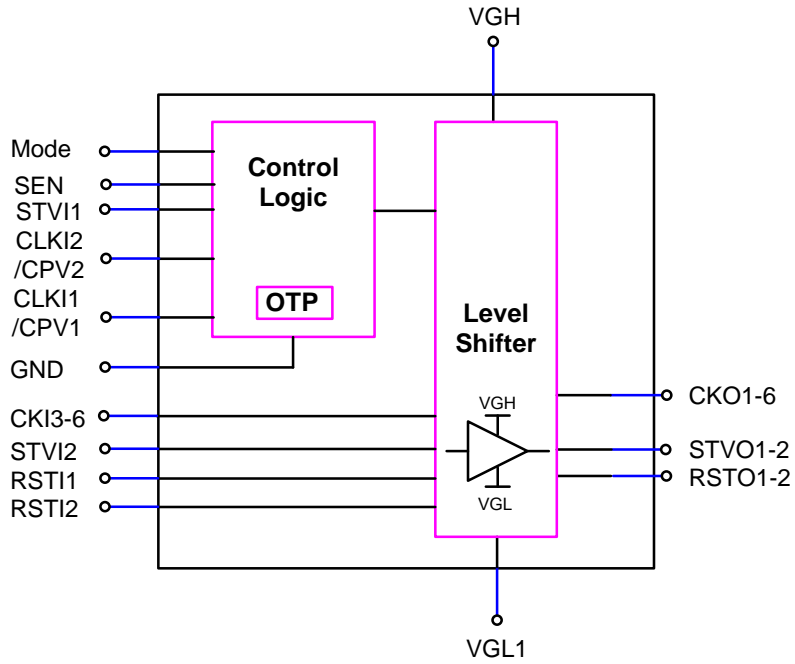


Figure 3. Function Block Diagram





Functional Pin Description

Pin NO.	Pin Name	Description
1	CKO5	Level shifter output.
2	CKO6	Level shifter output.
3	STVO1	Level shifter output.
4	RSTO1	Level shifter output.
5	STVO2	Level shifter output.
6	RSTO2	Level shifter output.
7	GND	Gound.
8	VGH	Positive high supply. Connect this pin with 2.2uF ceramic capacitor to GND.
9	VGL1	Negative low supply 1. Connect this pin with 2.2uF ceramic capacitor to GND.
10	NC	Not connected pin.
11	NC	Not connected pin.
12	Mode	TCON mode selection pin. Internal pull-down resistance.
13	NC	Not connected pin.
14	SEN	Sense Voltage pin.
15	RSTI2	Level shifter input. Internal pull-down resistance.
16	RSTI1	Level shifter input. Internal pull-down resistance.
17	STVI2	Level shifter input. Internal pull-down resistance.
18	CKI6	Level shifter input. Internal pull-down resistance.
19	CKI5	Level shifter input. Internal pull-down resistance.
20	CKI4	Level shifter input. Internal pull-down resistance.
21	CKI3	Level shifter input. Internal pull-down resistance.
22	CKI2/CPV2	Level shifter input. Internal pull-down resistance.
23	CKI1/CPV1	Level shifter input. Internal pull-down resistance.
24	STVI1	Level shifter input. Internal pull-down resistance.
25	CKO1	Level shifter output.
26	NC	Not connected pin.
27	CKO2	Level shifter output.
28	NC	Not connected pin.
29	CKO3	Level shifter output.
30	NC	Not connected pin.
31	CKO3	Level shifter output.
32	NC	Not connected pin.
EP		Connect to VGL. The copper area of the ground plane must be large enough to ensure adequate thermal performance.



Absolute Maximum Ratings ^{Note 1}

◇	STVI1, STVI2, RSTI1, RSTI2, SEN, Mode, to GND	-----	-0.3V to +7V
◇	CKI1/CPV1, CKI2/CPV2, CKI3, CKI4, CKI5, CKI6 to GND	-----	-0.3V to +7V
◇	VGH to GND	-----	-0.3V to +45V
◇	VGL1 to GND	-----	-20V to +0.3V
◇	CKO1, CKO2, CKO3, CKO4, CKO5, CKO6 to VGL1	-----	-0.3V to +60V
◇	STVO1, STVO2, RSTO1, RSTO2 to VGL1	-----	-0.3V to +60V
◇	Operating Junction Temperature Range (T _J)	-----	-40 °C to +150°C
◇	Operation Ambient Temperature Range	-----	-40°C to +85°C
◇	Storage Temperature Range	-----	-65°C to +150°C
◇	Maximum Soldering Temperature (at leads, 10sec)	-----	+260°C
◇	Maximum Junction Temperature	-----	+150°C

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

◇	Thermal Resistance		
	TQFN-32 4x4, θ_{JA}	-----	46.8°C/W
	TQFN-32 4x4, θ_{JC}	-----	19.5°C/W





Electrical Characteristics

$V_{GH}=25V$, $V_{GL1}=-10V$, $T_A=25^\circ C$, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
General						
VGH Input Range	V_{GH}		16		45	V
VGL1 Input Range	V_{GL1}		-20		-3	V
Supply Current	I_{GH}	STVix=RSTIx=CKIx=0V			1	mA
	I_{GL1}	STVix=RSTIx=CKIx=0V	-0.5			mA
UVLO Rising Threshold	V_{UVLO}	V_{GH} Rising	14	15	16	V
UVLO Falling Threshold		V_{GH} Falling	2	3.5	5	V
Thermal Shutdown Threshold	T_{SD}	Temperature Rising	130	150	170	$^\circ C$
Control Signals (SEN, Mode)						
SEN	V_{SEN}				0.8	V
			2			
Mode	V_{TCON}	TCON Mode 0			0.8	V
		TCON Mode 1	2			
Mode Pull Down Resistor	R_{PD_TCON}		50	100	200	k Ω
Level Shifters (STVx, RSTx)						
Level Shifter Input Threshold	V_{IL}	STVix, RSTIx Falling			0.8	V
	V_{IH}	STVix, RSTIx Rising	2			
Pull Down Resistor	R_{PD}	STVix, RSTIx	50	100	200	k Ω
High Side On Resistance	R_{DS_H}			30	60	Ω
Low Side On Resistance	R_{DS_L}			15	30	
Slew Rate	T_R	$C_{OUT}=4.7nF$, From 20% to 80%	20			V/us
	T_F	$C_{OUT}=4.7nF$, From 80% to 20%	30			
Propagation Delay	T_{R_dly}	$C_{OUT}=150pF$, V_{OUT} Rising		40	100	ns
	T_{F_dly}	$C_{OUT}=150pF$, V_{OUT} Falling		50	100	



Electrical Characteristics (Continued)

$V_{GH}=25V$, $V_{GL1}=V_{GL2}=-10V$, $T_A=25^{\circ}C$, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Level Shifters (CKx)						
Operating Frequency	Freq	CPV1, CPV2			500	kHz
Level Shifter Input Threshold	V_{IL}	CKIx Falling			0.8	V
	V_{IH}	CKIx Rising	2			
Pull Down Resistor	R_{PD}	CKIx	50	100	200	k Ω
High Side On Resistance	R_{DS_H}			11	25	Ω
Low Side On Resistance	R_{DS_L}			7	15	Ω
Slew Rate	T_R	$C_{OUT}=4.7nF$, From 20% to 80%	50			V/us
	T_F	$C_{OUT}=4.7nF$, From 80% to 20%	50			
Propagation Delay	T_{R_dly}	$C_{OUT}=150pF$, V_{OUT} Rising		40	100	ns
	T_{F_dly}	$C_{OUT}=150pF$, V_{OUT} Falling		50	100	





Timing Diagram-Power On/ Off Sequence

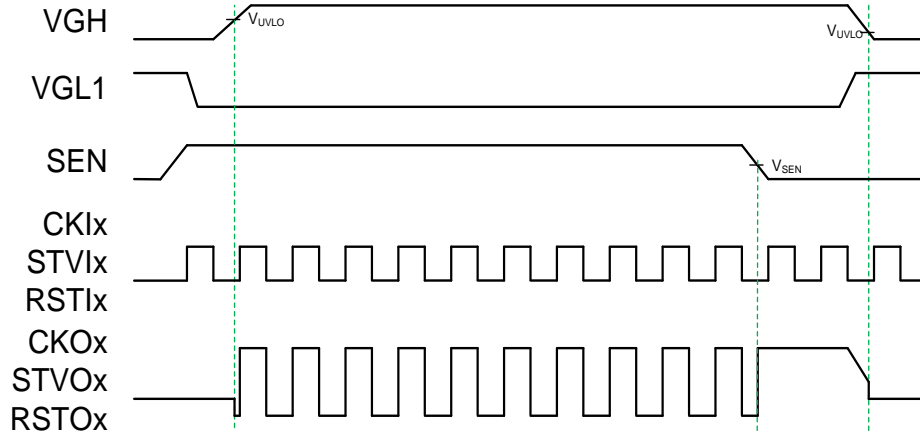


Figure 4. Power Sequence with normal control





Timing Diagram-TCON Mode0

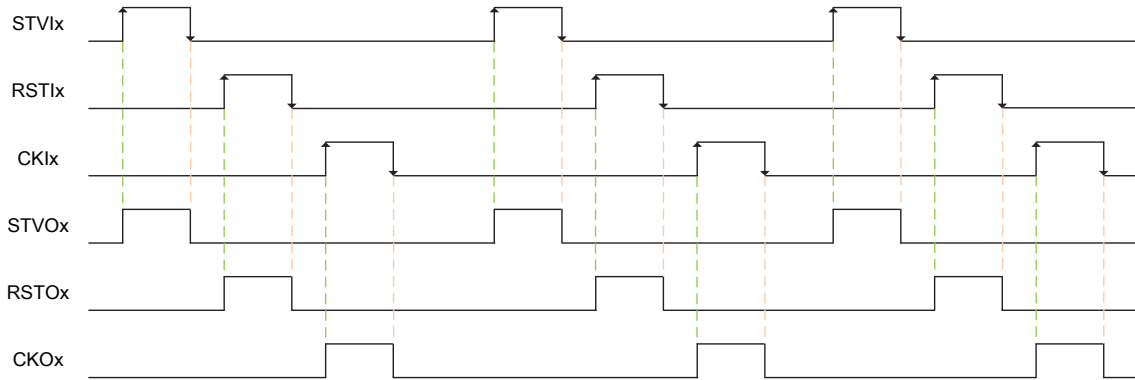


Figure 5. TCON Mode0

TCON Mode0 Description:

1. STVix↑ / RSTix↑ / CKIx↑ @ STVOx↑ / RSTOx↑ / CKOx↑;
2. STVix↓ / RSTix↓ / CKIx↓ @ STVOx↓ / RSTOx↓ / CKOx↓;

Timing Diagram-TCON Mode1

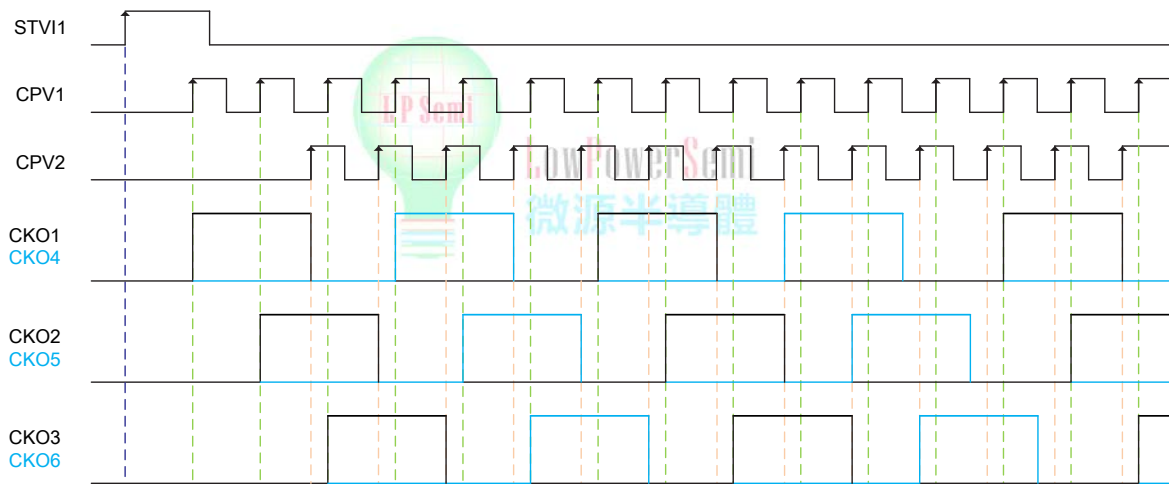


Figure 6. Power Sequence and GPM Control

TCON Mode1 Description:

1. TCON input signals are STVI1, CPV1, CPV2.
2. When STVIN1 is rising, all CKOx must be pull low; until CPV1 is rising edge, CKOx could active.
3. CPV1 rising edge will decide six CKOx rise location, and CPV2 rising edge will decide six CKOx fall locaton.



Application Information

The LP6297B is level shifter for TFT LCD panel in GOP application. The device has six clock outputs, two STV outputs, two RST outputs. The clock output supports normal TCON application and CPV input application which can save TCON output value.

Under Voltage Lockout (UVLO)

The LP6297B had an UVLO internal circuit that enable the device once the voltage on the VGH voltage exceeds the UVLO threshold voltage.

TCON Mode Selection

The device supports two TCON modes.

TCON mode 0:	level shifter follows STV1x/RST1x/CK1x. It converts signal to higher/lower level signal.
TCON mode 1:	Decode CPV1 and CPV2 signal to generate the higher/lower level output. The rising edge of CPV1 decides CKOx rising location, and the rising edge of CPV2 decides CKOx falling location.

Refer to figure 5 and figure 6 for TCON mode timing.

Over Temperature Protection

The LP6297B device enters over temperature protection(OTP) if its junction temperature exceeds 150°C (Typ.). Then all the outputs will be high impedance and the IC will latch-up. VGH must be cycled to recover normal operation.

Short Circuit Protection

During normal operation, if level shifter output (include CKOx, STVOx, RSTOx) short to VGH, VGL1 or GND, the short circuit protection will be detected. When the state happens, all the outputs will be high impedance and the IC will latch-up. VGH must be cycled to recover normal operation.

Layout Guideline

The output stages of the LP6297B are capable of sinking and sourcing high peak currents and care must be taken during PCB layout to ensure that this performance. In particular, the change of current at the rising and falling edges of each output require stray inductance to be minimized. It is easily solved by routing the output signals using short, wide PCB tracks and using a low impedance ground plane on the other side of the board to conduct return currents. Tracks between the decoupling capacitors and the corresponding power supply pins should also be keeping short and wide as possible.

1. The input capacitor should be located as closed as possible to the VGH, VGL and ground plane.
2. Minimize the distance of all traces connected to the Output node, that the traces short and wide route to obtain optimum performance.

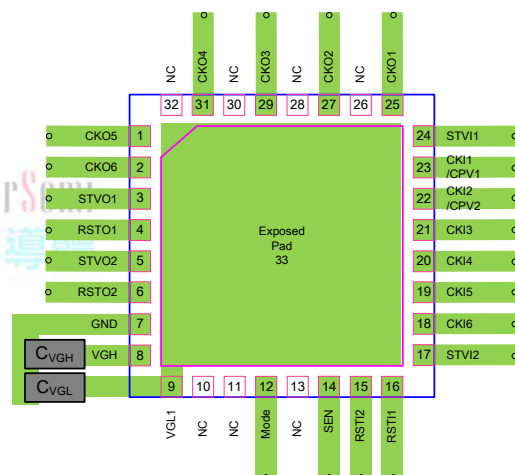
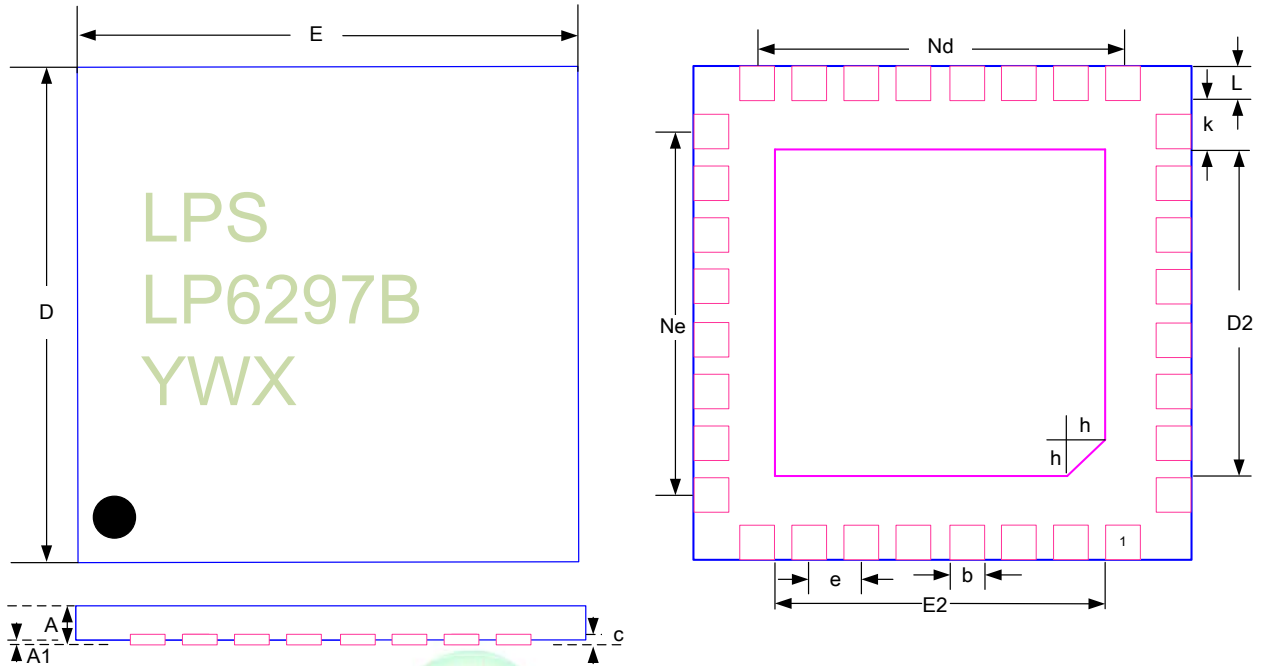


Figure 7. Recommended PCB Layout Diagram



Outline Information

TQFN-32 Package (4x4) pitch 0.4 (Unit: mm)



SYMBOL	DIMENSION IN MILLIMETER		
	MIN	NOM	MAX
A	0.700	0.750	0.800
A1	---	0.020	0.050
b	0.150	0.200	0.250
c	0.180	0.200	0.250
D	3.900	4.000	4.100
D2	2.600	2.650	2.700
E	3.900	4.000	4.100
E2	2.600	2.650	2.700
K	0.200	---	---
e	0.400 BSC		
Nd	2.800 BSC		
Ne	2.800 BSC		
L	0.350	0.400	0.450
h	0.300	0.350	0.400