



600KHz, 16V/2A Synchronous Step-down Converter

General Description

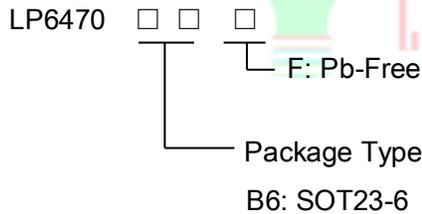
The LP6470 contains an independent 600KHz constant frequency, current mode, PWM step-down converters. The converter integrates a main switch and a synchronous rectifier for high efficiency without an external Schottky diode. The LP6470 is ideal for powering portable equipment that runs from a 2cell Lithium-Ion (Li+) battery. The converter can supply 2000mA of load current from a 3.5V to 16V input voltage. The output voltage can be regulated as low as 0.8V.

The LP6470 is available in a SOT23-6 package and is rated over the -40°C to 85°C temperature range.

Features

- ◆ Input Voltage Range: 3.5V to 16V
- ◆ Output Voltage Range: 0.8V to 12V
- ◆ 2000mA Load Current on Channel
- ◆ Up to 96% Efficiency
- ◆ <6uA Shutdown Current
- ◆ 600KHz Switching Frequency
- ◆ Short Circuit Protection
- ◆ Thermal Fault Protection
- ◆ SOT23-6 Package
- ◆ RoHS Compliant and 100% Lead (Pb)-Free

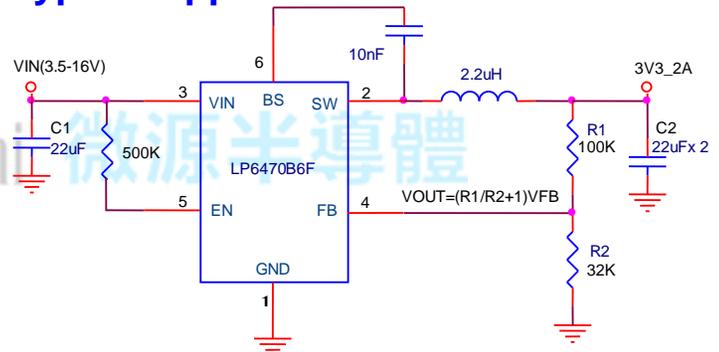
Order Information



Applications

- ✧ Portable Media Players
- ✧ Cellular and Smart mobile phone
- ✧ PDA/DSC
- ✧ GPS Applications

Typical Application Circuit



The C1 must be as close as possible to the chip, and the capacitor loop is the same.

Marking Information

Device	Marking	Package	Shipping
LP6470	LPS A8YWX	SOT23-6	3K/REEL
Y: Year code. W: Week code. X: Batch numbers.			



Functional Pin Description

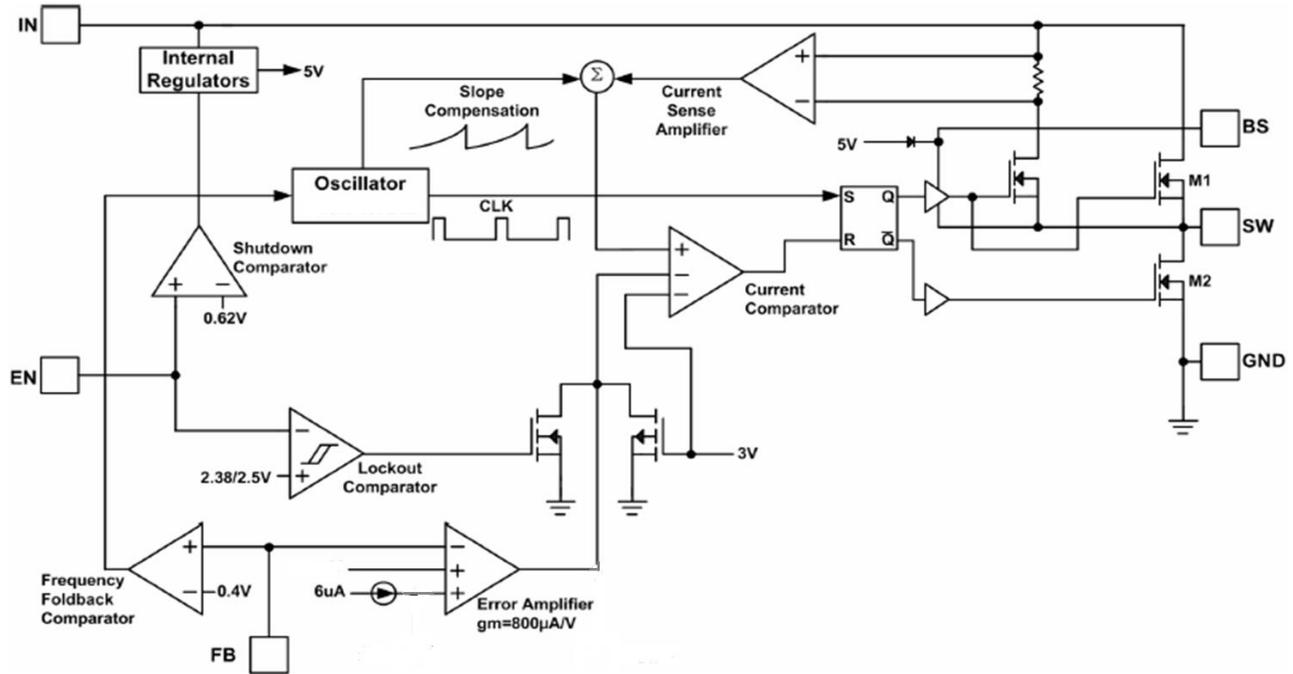
Package Type	Pin Configurations
SOT23-6	<p style="text-align: center;">Top View</p>

Pin Description

Pin	Name	Description
1	GND	Ground.
2	SW	Switch Mode Connection to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.
3	VIN	Voltage supply.
4	FB	Feedback Input. Connect FB to the center point of the external resistor divider. Normal voltage for this pin is 0.8V.
5	EN	Enable Control Input. Drive EN above 1.8V to turn on the Channel. Drive EN below 0.4V to turn it off.
6	BS	High-Side Gate Drive Boost Input. Connect a 0.01uF or greater capacitor from SW to BS to power the high side switch.



Function Diagram



Absolute Maximum Ratings ^{Note 1}

- ✧ Input voltage to GND ----- -0.3V to 24V
- ✧ SW voltage to GND ----- -0.3V to 24V
- ✧ BS voltage to GND ----- -0.3V to 24V
- ✧ VEN voltage to GND ----- -0.3V to 24V
- ✧ VFB voltage to GND ----- -0.3V to 6.5V
- ✧ Maximum Junction Temperature ----- 150°C
- ✧ Storage Temperature ----- -45°C to 165°C
- ✧ Operating Ambient Temperature Range ----- -40°C to 85°C
- ✧ Maximum Soldering Temperature (at leads, 10 sec) ----- 260°C

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

- ✧ Maximum Power Dissipation (SOT23-6, PD, T_A=25°C) ----- 0.45W
- ✧ Thermal Resistance (SOT23-6, θ_{JA}) ----- 250°C/W

ESD Susceptibility

- ✧ HBM(Human Body Mode) ----- 2KV
- ✧ MM(Machine Mode) ----- 200V



Electrical Characteristics

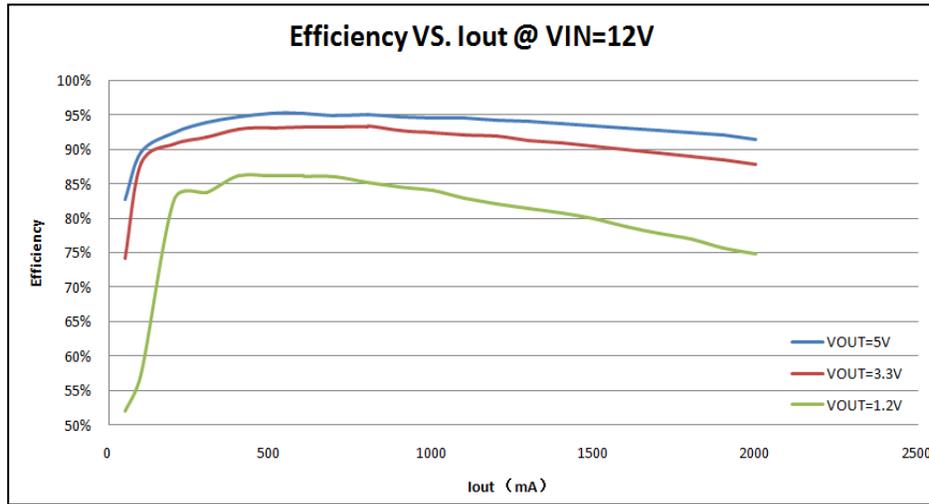
$V_{IN}=12V$, $V_{EN}=5V$, $T_A=25^{\circ}C$, unless otherwise noted

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IN}	Input Voltage		3.5		16	V
V_{OUT}	Output Voltage Range		0.8		12	V
I_Q	Quiescent Current	$V_{FB}=0.9V$		450	900	μA
I_{SHDN}	Shutdown Current	$V_{EN}=GND$			6	μA
I_{LIM}	High-Side N-Channel Current Limit		3			A
$R_{DS(ON)H}$	High-Side Switch On Resistance			100		m Ω
$R_{DS(ON)L}$	Low-Side Switch On Resistance			80		m Ω
$\Delta V_{Line-reg}/\Delta V_{IN}$	Line Regulation	$V_{IN}=4.5V$ to 12V		0.2		%/V
V_{FB}	Feedback Threshold Voltage Accuracy	$16V > V_{IN} > 4.5V$	0.784	0.8	0.816	V
I_{FB}	FB Leakage Current	$V_{FB}=1.0V$			30	nA
f_{OSC}	Oscillator Frequency			600		KHz
T_{SD}	Over-Temperature Shutdown Threshold			150		$^{\circ}C$
T_{HYS}	Over-Temperature Shutdown Hysteresis			20		$^{\circ}C$
V_{INOVP}	Over Voltage Protection Threshold			18		V
$V_{INOVP-HYS}$	Over Voltage Protection Hysteresis			1		V
V_{INUV}	Under voltage Lockout Threshold			3.3		V
$V_{INUV-HYS}$	Under voltage Lockout Hysteresis			0.3		V
D_{MAX}	Maximal duty cycle				95	%
$V_{EN(L)}$	Enable Threshold Low				0.4	V
$V_{EN(H)}$	Enable Threshold High		1.8			V
I_{EN}	Input Low Current	$V_{IN}=V_{EN}=5V$		4		μA

Note: Output Voltage: $V_{OUT} = V_{FB} \times (1 + R_1 / R_2)$ Volts;

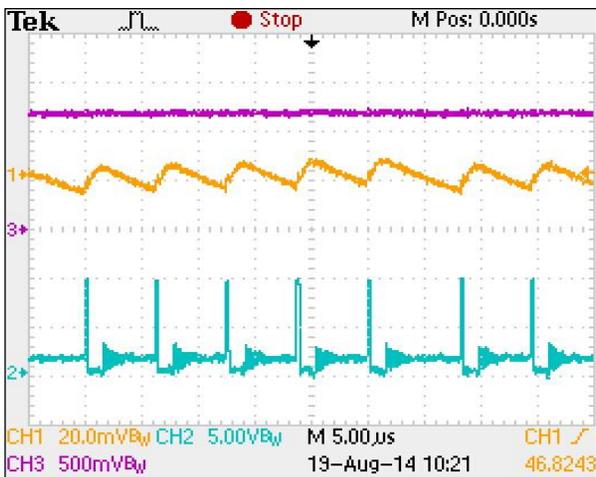


Typical Operating Characteristics



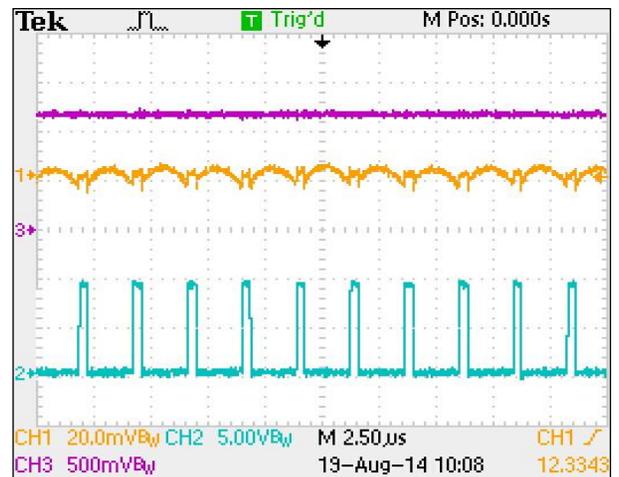
Output Wave

Output Wave



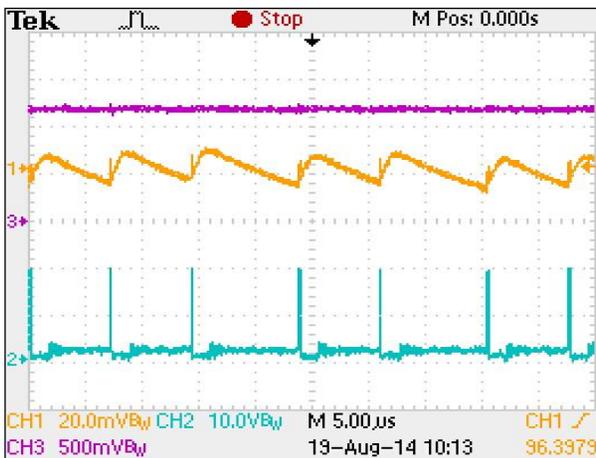
VIN=9V, VOUT=1.2V, IOUT=50mA

(CH1=VOUTPP, CH2=Vsw, CH3=VOUT)



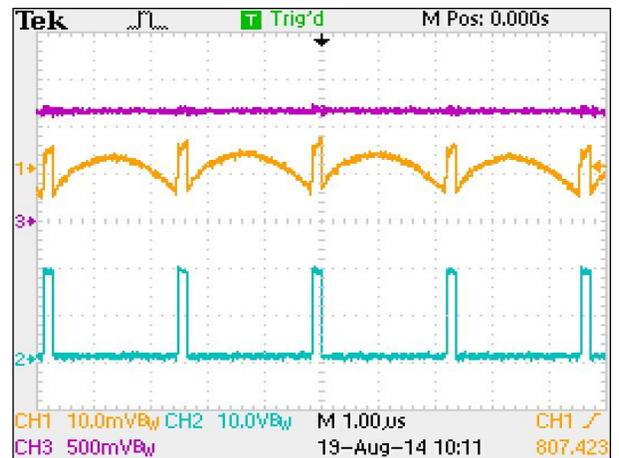
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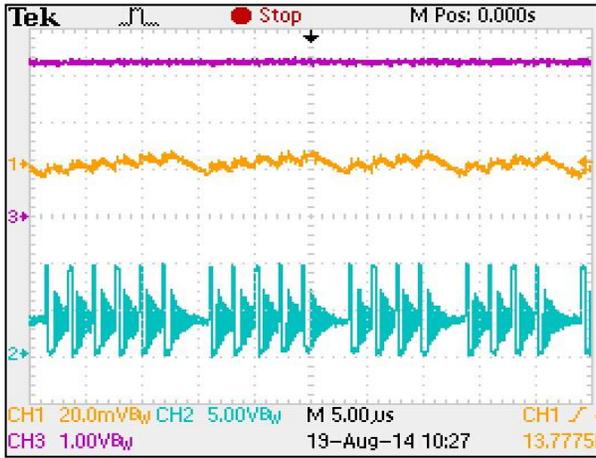


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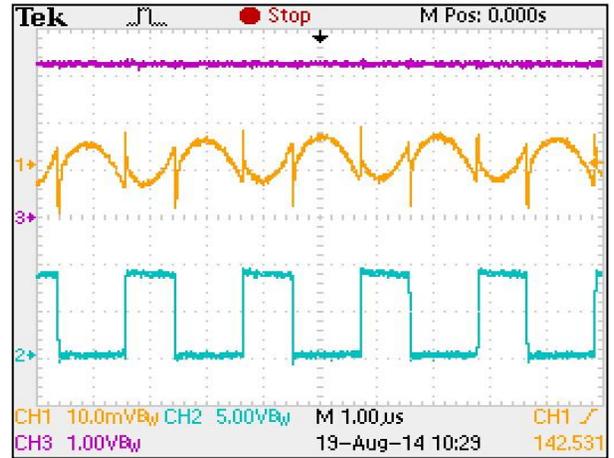
Output Wave



V_{IN}=9V, V_{OUT}=3.3V, I_{OUT} =50mA

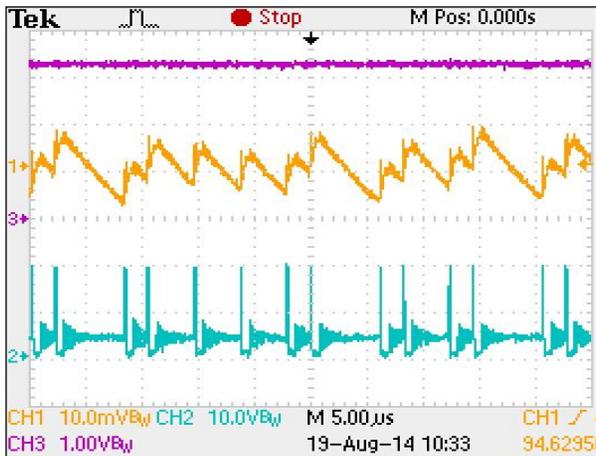
(CH1=V_{OUTPP}, CH2= V_{sw}, CH3=V_{OUT})

Output Wave



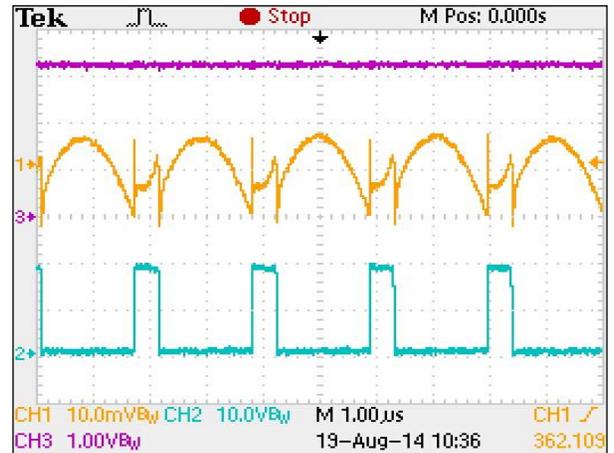
V_{IN}=9V, V_{OUT}=3.3V, I_{OUT} =2.0A

(CH1=V_{OUTPP}, CH2= V_{sw}, CH3=V_{OUT})



V_{IN}=12V, V_{OUT}=3.3V, I_{OUT} =50mA

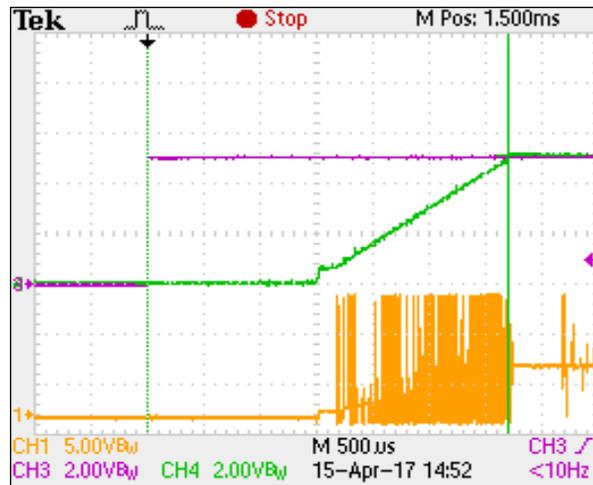
(CH1=V_{OUTPP}, CH2= V_{sw}, CH3=V_{OUT})



V_{IN}=12V, V_{OUT}=3.3V, I_{OUT} =2.0A

(CH1= V_{OUTPP}, CH2= V_{sw}, CH3=V_{OUT})

Start up



CH1= V_{sw}, CH3=V_{EN}, CH4=V_{OUT}



General Description

Functional Description

The LP6470 is a high output current monolithic switch-mode step-down DC-DC converter. The device operates at a fixed 600KHz switching frequency, and uses a slope compensated current mode architecture. This step-down DC-DC converter can supply up to 2A output current at input voltage range from 3.5V to 16V. It minimizes external component size and optimizes efficiency at the heavy load range. The integrated slope compensation allows the device to remain stable over a wider range of inductor values so that smaller values (2.2µH to 10µH) with lower DCR can be used to achieve higher efficiency. The device can be programmed with external feedback to any voltage, ranging from 0.8V to 12V. It uses internal MOSFETs to achieve high efficiency and can generate very low output voltages by using an internal reference of 0.8V. At dropout, the converter duty cycle increases to 95% and the output voltage tracks the input voltage minus the low $R_{DS(ON)}$ drop of the P-channel high-side MOSFET and the inductor DCR. The internal error amplifier and compensation provides excellent transient response, load and line regulation.

Enable The Chip

The enable pin is active high. When pulled low, the enable input (EN) forces the LP6470 into a low-power, non-switching state. The total input current during shutdown is less than 1µA. When apply LP6470 to a circuit, there should be a 100KΩ resistance between EN and GND.

Current Limit and Over-Temperature Protection

For overload conditions, the peak input current is limited to 3A. To minimize power dissipation and stresses under current limit and short-circuit conditions, switching is terminated after entering current limit condition. The termination lasts for seven consecutive clock cycles after a current limit has been sensed during a series of four consecutive periods of oscillations. Thermal protection completely disables switching when internal dissipation becomes excessive. The junction over-temperature threshold is 150°C with 20°C of hysteresis. Once an over-temperature or over-current fault conditions is removed, the output voltage automatically recovers.

Dropout Operation

When input voltage decreases near the value of the output voltage, the LP6470 allows the main switch to remain on for more than one switching cycle and increases the duty cycle until it reaches 95%. The duty cycle D of a step-down converter is defined as:

$$D = t_{ON} \times f_{OSC} \times 100\% = \frac{V_{OUT}}{V_{IN}} \times 100\%$$

Where T_{ON} is the main switch on time and f_{osc} is the oscillator frequency.

Setting the Output Voltage

The LP6470 can be externally programmed. Feedback resistors R_1 and R_2 program the output to regulate at a voltage higher than 0.8V. Although a larger value will further reduce quiescent current, it will also increase the impedance of the feedback node, making it more sensitive to external noise and interference. For achieving circuit loop stability, the R_1 must be between 50K and 900K. The LP6470, combined with an external feed forward capacitor, delivers enhanced transient response for extreme pulsed load applications. The addition of the feed forward capacitor typically requires a larger output capacitor C_2 for stability. The external resistor sets the output voltage according to the following equation:

$$V_{OUT} = 0.8V \times \left(1 + \frac{R_1}{R_2}\right)$$

$$R_1 = \left(\frac{V_{OUT}}{0.8V} - 1\right) \times R_2$$

Table1 shows the resistor selection for different output voltage settings

V_{OUT} (V)	R_1 (KΩ)	R_2 (KΩ)
1.1	100	266.7
1.2	100	200.0
1.3	100	160.0
1.4	100	133.3
1.5	100	114.3
1.8	100	80.0
1.85	100	76.2
2.0	100	66.7
2.5	100	47.1
3.3	100	32.0

Table1: Resistor Selections for Different Output Voltage Settings (Standard 1% Resistors Substituted For Calculated Values).



Output Capacitor Selection

The function of output capacitance is to store energy to attempt to maintain a constant voltage. The energy is stored in the capacitor's electric field due to the voltage applied. The value of output capacitance is generally selected to limit output voltage ripple to the level required by the specification. Since the ripple current in the output inductor is usually determined by L , V_{OUT} and V_{IN} , the series impedance of the capacitor primarily determines the out-put voltage ripple. The three elements of the capacitor that contribute to its impedance (and output voltage ripple) are equivalent series resistance (ESR), equivalent series inductance (ESL), and capacitance (C). The output voltage droop due to a load transient is dominated by the capacitance of the ceramic output capacitor. During a step increase in load current, the ceramic output capacitor alone supplies the load current until the loop responds. Within three switching cycles, the loop responds and the inductor current increases to match the load current demand. The relationship of the output voltage droop during the three switching cycles to the output capacitance can be estimated by:

$$C_{OUT} = \frac{3 \times \Delta I_{LOAD}}{V_{DROOP} \times f_S}$$

In many practical designs, to get the required ESR, a capacitor with much more capacitance than is needed must be selected. For continuous or discontinuous inductor current mode operation, the ESR of the C_{OUT} needed to limit the ripple to ΔV_{OUT} , V peak-to-peak is:

$$ESR \leq \frac{\Delta V_{OUT}}{\Delta I_L}$$

Ripple current flowing through a capacitor's ESR causes power dissipation in the capacitor. This power dissipation causes a temperature increase internal to the capacitor. Excessive temperature can seriously shorten the expected life of a capacitor. Capacitors have ripple current ratings that are dependent on ambient temperature and should not be exceeded. The output capacitor ripple current is the inductor current, I_L , minus the output current, I_{OUT} .

Inductor Selection

For most designs, the LP6470 operates with inductor values of 2.2 μ H to 10 μ H. Low inductance values are physically smaller but require faster switching, which results in some efficiency loss. The inductor value can be derived from the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is inductor ripple current. Large value inductors lower ripple current and small value inductors result in high ripple currents. Choose inductor ripple current approximately 60% of the maximum load current 2A, or

$$\Delta I_L = 1200\text{mA}$$

Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR.

Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor. For optimum voltage-positioning load transients, choose an inductor with DC series resistance in the 20m Ω to 100m Ω range. For higher efficiency at heavy loads (above 200mA), or minimal load regulation (but some transient overshoot), the resistance should be kept below 100m Ω . The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation (2A + 600mA).



Thermal Calculations

There are three types of losses associated with the LP6470 step-down converter: switching losses, conduction losses, and quiescent current losses. Conduction losses are associated with the $R_{DS(ON)}$ characteristics of the power output switching devices. Switching losses are dominated by the gate charge of the power output switching devices.

At full load, assuming continuous conduction mode (CCM), a simplified form of the losses is given by:

$$P_{TOTAL} = \frac{I_{OUT}^2 (R_{DS(ON)(HS)} \times V_{OUT} + R_{DS(ON)(LS)} \times (V_{IN} - V_{UTO}))}{V_{IN}} + (t_{SW} \times f \times I_{OUT} + I_Q) \times V_{IN}$$

I_Q is the step-down converter quiescent current. The term t_{sw} is used to estimate the full load step-down converter switching losses.

For the condition where the step-down converter is in dropout at 95% duty cycle, the total device dissipation reduces to:

$$P_{TOTAL} = I_{OUT}^2 \times R_{DS(ON)(HS)} + I_Q \times V_{IN}$$

Since $R_{DS(ON)}$, quiescent current, and switching losses all vary with input voltage, the total losses should be investigated over the complete input voltage range. Given the total losses, the maximum junction temperature can be derived from the θ_{JA} for the SOT23-6 package which is 250°C/W.

$$T_{J(MAX)} = P_{TOTAL} \times \theta_{JA} + T_{AMB}$$

Layout Guidance

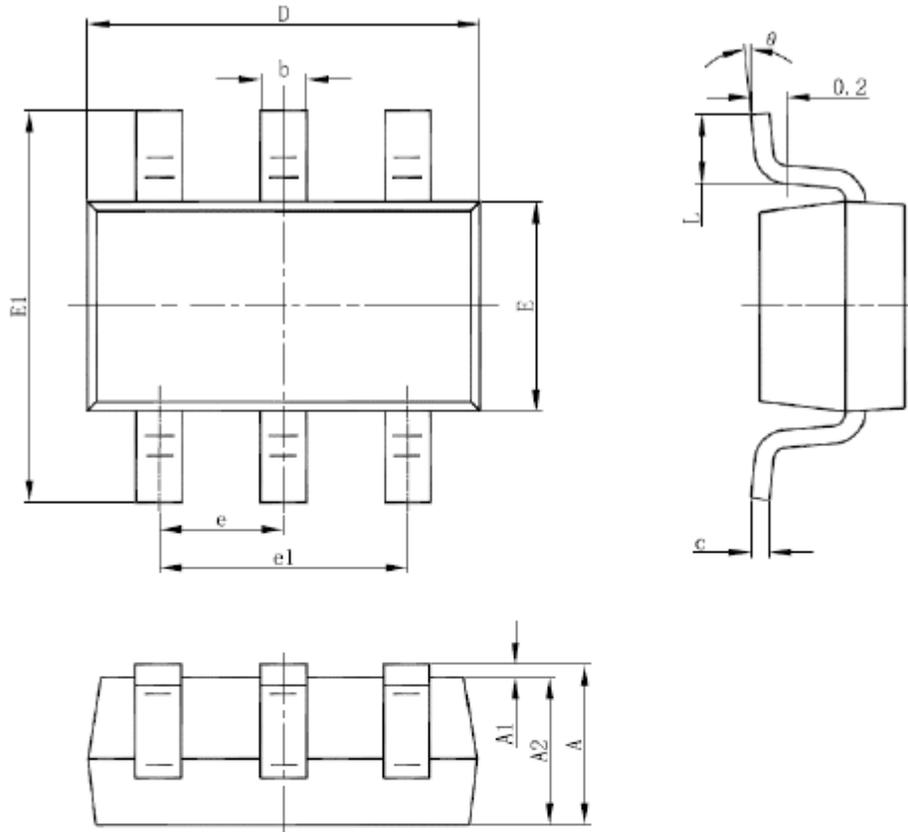
When laying out the PC board, the following layout guideline should be followed to ensure proper operation of the LP6470:

1. The power traces, including the GND trace, the SW trace and the IN trace should be kept short, direct and wide to allow large current flow. The L connection to the SW pins should be as short as possible. Use several VIA pads when routing between layers.
2. The input capacitor (C_{IN}) should connect as closely as possible to VIN (Pin 5) and GND to get good power filtering.
3. Keep the switching node, SW (Pins 6) away from the sensitive FB/OUT node.
4. The feedback trace or OUT pin should be separate from any power trace and connect as closely as possible to the load point. Sensing along a high-current load trace will degrade DC load regulation.
5. The output capacitor C_{OUT} and L should be connected as closely as possible. The connection of L to the SW pin should be as short as possible and there should not be any signal lines under the inductor.
6. The resistance of the trace from the load return to PGND should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.



Packaging Information

SOT-23-6 Package Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°